

Study of the V_{th} shift of the thin-film transistor by the bias temperature stress test

by Y. Fujimoto

Amorphous silicon thin-film transistors (a-Si:H TFTs) are now widely used as the switching device in the active-matrix addressing of liquid crystal displays. One concern is the potential instability problems associated with the threshold voltage (V_{th}) shifts to higher values after prolonged operating times. The reason for this V_{th} shift has been widely discussed, and two models accounting for it have been suggested. One model explains the shifts by the trapping of electrons in the insulator, the other model by the creation of the metastable states at the a-Si:H/ SiN_x interface. Our TFT insulator has the rather complicated structure of an anodic oxide film, SiO_x , SiN_x sequentially stacked over the gate electrode, which makes it difficult to separate the contribution of each layer. To confirm the V_{th} shift mechanism and the contribution of each layer of insulator to the V_{th} shift, we have prepared samples with a

series of different insulators and have measured the bias dependence of their V_{th} shifts. Our results show that the anodic oxide film makes no contribution to the V_{th} shift, and it makes little difference to the V_{th} shift whether the next insulator is SiN_x or SiO_x . The latter fact may be explained in two ways. One is that both SiN_x and SiO_x make the same contribution to the V_{th} shift. Alternatively, neither SiN_x nor SiO_x makes any contribution to the V_{th} shift, but the a-Si:H/gate insulator interface has some contribution. From these experiments, it cannot be determined which of the proposed mechanisms is consistent with the behavior of the V_{th} shift of our a-Si:H TFT.

Introduction

In recent years, amorphous silicon thin-film transistors (a-Si:H TFTs) have received widespread attention in the

©Copyright 1992 by International Business Machines Corporation. Copying in printed form for private use is permitted without payment of royalty provided that (1) each reproduction is done without alteration and (2) the *Journal* reference and IBM copyright notice are included on the first page. The title and abstract, but no other portions, of this paper may be copied or distributed royalty free without further permission by computer-based and other information-service systems. Permission to *republish* any other portion of this paper must be obtained from the Editor.

active-matrix addressing of liquid crystal displays. However, the a-Si:H TFT has an instability problem in that a threshold voltage (V_{th}) shift occurs after the prolonged application of the gate voltage (V_g). It has been proposed that this instability should be attributed to the trapping of electrons by states in the insulator [1] or to the creation of the metastable states at the a-Si:H/SiN_x interface by weak Si-Si bonds being broken due to capture of the excess electrons [2-4].

The TFT used in our arrays was fabricated with an inverted staggered-electrode configuration in which the insulator is deposited over the gate electrode. This insulator has a very complicated structure. After the anodic oxide (AO) film was created by the anodizing oxidation of the upper region of the gate electrode, SiO_x and SiN_x were deposited sequentially on it by plasma-enhanced chemical vapor deposition (PECVD). It is not yet clear which region of AO, SiO_x, SiN_x, or the a-Si:H/SiN_x interface, contributes to the V_{th} shift. This paper describes the experimental method and results used to try to identify the mechanism and the region contributing to the V_{th} shift by a bias temperature stress (BTS) test.

Sample preparation

As shown in Table 1, seven samples with different gate insulator structures were fabricated. Sample A is a standard one which is commonly used in IBM liquid crystal displays. In addition, six samples with different structures and thicknesses of SiN_x and/or SiO_x were prepared. Samples E and G were fabricated with only a single insulator. This was aimed at identifying the region of the SiN_x or SiO_x layer in which more electrons were trapped. Samples A, C, D, and F were fabricated with an AO film, while samples B, E, and G were fabricated without this film. This was intended to confirm whether the electrons were trapped in the AO film.

The thickness of each film was determined such that all samples had the same gate capacitance, so that the induced charge in the channel had the same value when the TFT was in the ON state. As shown in Figure 1, these insulators, a-Si:H (2500 Å) and P-doped n⁺ a-Si:H (500 Å) were successively deposited by PECVD. Finally, the SiO_x (2000 Å)/SiN_x (1000 Å) as a passivation layer was deposited after the n⁺ a-Si:H was etched off the channel region.

BTS test and the V_{th} shift mechanism

To simulate the V_{th} shift of long time periods in a relatively short experimental time period, the BTS experiment was performed by the application of a dc gate voltage under high temperature. Before the TFT was subjected to the bias stress, the source-drain current I_{ds} vs. gate voltage V_g (I_d - V_g) characteristics, as shown in Figure 2, were

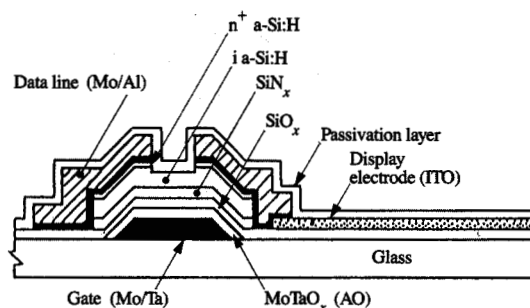


Figure 1

Cross section of amorphous silicon TFT (back channel cut type).

Table 1 Samples with different insulator structures.

Sample	SiN _x (Å)	SiO _x Å	AO (Å)
A	2000	1000	1500
B	2000	1000	0
C	500	2000	1500
D	3500	0	1500
E	3500	0	0
F	0	2000	1500
G	0	2000	0

measured at a drain voltage V_d of 10 V. Then, as shown in Figure 3, the TFT was heated with the source, drain, and gate electrodes all grounded to prevent any shift in V_{th} . When the temperature reached a certain high value, a positive dc gate voltage (+BTS) was applied to the TFT with the drain and source electrodes grounded. Then the TFT was cooled to room temperature with all electrodes grounded, and the I_d - V_g characteristic was remeasured.

As shown in Figure 2, V_{th} was defined as the intersection of the square root of the I_d curve to the V_g axis. The V_{th} shift is defined as

$$\Delta V_{th} = V_{th2} - V_{th1} \quad (1)$$

where V_{th1} is the threshold voltage before stress and V_{th2} is the threshold voltage after stress. The V_{th} shift had a strong dependency on temperature, gate voltage, and stress time, and approximately followed the empirical equation [5]

$$\Delta V_{th} = A \exp \left(-\frac{E_a}{kT} \right) (V_g)^\alpha (\log t)^\beta \quad (2)$$

where A is a constant, k is the Boltzmann constant, T is the absolute temperature, E_a is an activation energy, V_g is the applied gate voltage, t is the stress time, and α and β

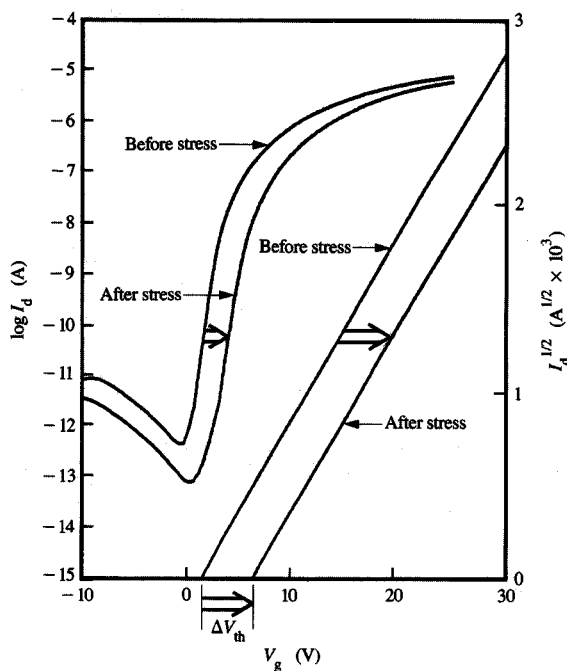


Figure 2

I_d - V_g characteristics before and after stress.

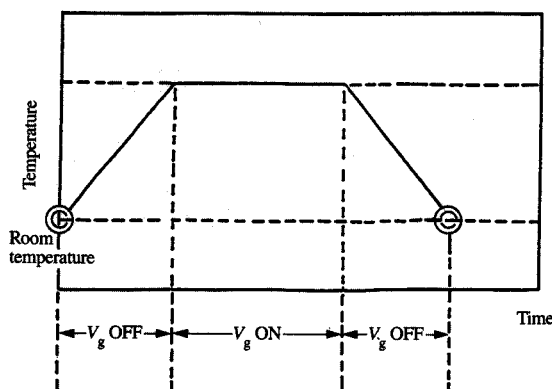


Figure 3

Schematic diagram of temperature and V_g by BTS.

are variables depending on the properties of the a-Si:H and the insulator.

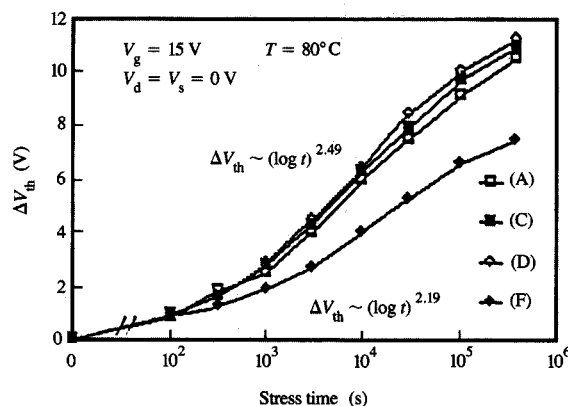
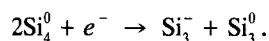


Figure 4

ΔV_{th} as a function of stress time for different insulators, yielding a value for the parameter β . For identification of the samples, see Table 1.

These factors are closely related to the V_{th} shift mechanism; one model [1] suggests that when the positive gate voltage is applied, electrons are induced at the a-Si:H/SiN_x interface by the field-effect conduction band bending, which creates the conduction channel. Some of the induced electrons tunnel to the states at the Fermi level in the insulator. The tunneling electrons move deeply within the insulator by phonon-assisted hopping. In this case, the activation energy is thermal, which is necessary for the electrons to hop to the neighbor state [1]. This has some similarities to charge transfer by direct tunneling in thin-oxide MNOS memory transistors.

However, an alternative model has recently been proposed [2-4]. In this model, the V_{th} shift is attributed to the creation of the metastable states at the a-Si:H/SiN_x interface during the prolonged application of the gate voltage. This creation is similar to the Staebler-Wronski effect [7], in which Si dangling bonds are created as a result of illumination. In this case, when the excess electrons are populated at the a-Si:H/SiN_x interface, weak Si-Si bonds at the conduction-band tail are broken by capturing these electrons, as follows:



The symbol Si_4^0 corresponds to the state in which four sp^3 hybrid orbitals are fully occupied by electrons. The metastable states correspond to the negative silicon bond designated by the symbol Si_3^- , whose antibonding state is occupied by the electron. The neutral Si_3^0 dangling bonds created by the above process capture the second electron.

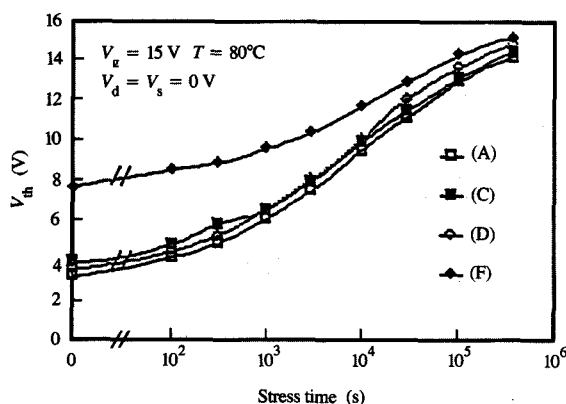


Figure 5

V_{th} as a function of stress time for different insulators. For identification of the samples, see Table 1.

In this case, the activation energy is also thermal, which is necessary for the creation of the metastable states.

The BTS experiment is performed by varying temperature, gate voltage, and stress time, not only to identify the contribution to the V_{th} shift of AO, SiO_x , SiN_x films or the Si:H/ SiN_x interface, but also to confirm that our TFTs have a behavior consistent with these models.

BTS experiment results

• Dependency of the V_{th} shift on stress time

As shown in Figure 4, a V_g of 15 V was applied to samples A, C, D, and F at 80°C for 100 h. These samples were all subjected to the anodizing oxidation. As shown in Table 1, samples A, C, and D were fabricated with a SiN_x layer. On the other hand, sample F was not fabricated with a SiN_x layer, but with a SiO_x layer. As a result, the V_{th} shifts of samples A, C, and D are equivalent, except that the V_{th} shift of sample F is smaller than any of the others. The reason for this phenomenon is explained as follows. As shown in Figure 5, the V_{th} of sample F before stress was higher than any of the others. This was because there existed more localized states at the a-Si:H/ SiO_x interface and thus more trapped electrons in the insulator. The former fact could be explained by the subthreshold behavior, in which the slope of the I_d - V_g characteristics for the TFT with SiO_x insulator was not as sharp as the one for the TFT with SiN_x or SiN_x/SiO_x insulator, as shown in Figure 6. This latter observation could be explained by the curve of the I_d - V_g characteristics for the TFT with SiO_x insulator, which shifted to the $+V_g$ direction, in contrast to

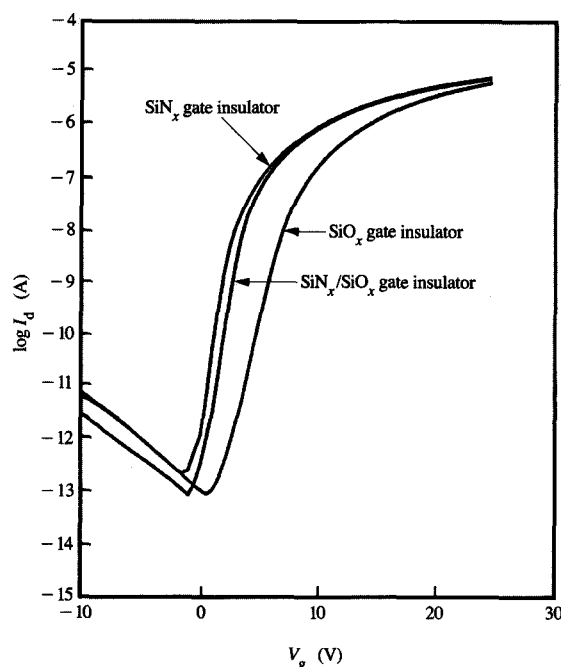


Figure 6

I_d - V_g characteristics before BTS for different gate insulators.

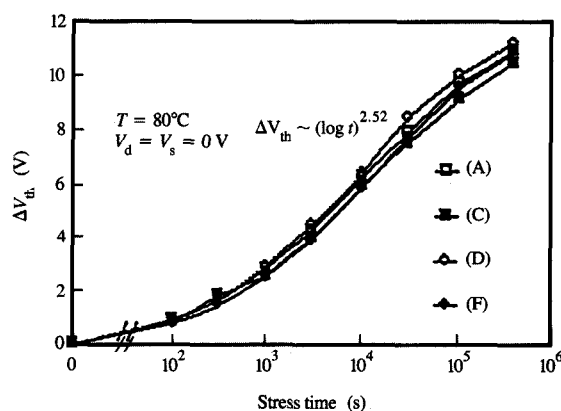


Figure 7

ΔV_{th} as a function of stress time for different insulators, yielding a value for the parameter β . V_g of 15 V is applied to samples A, C, and D, but V_g of 19 V is applied to sample F. For identification of the samples, see Table 1.

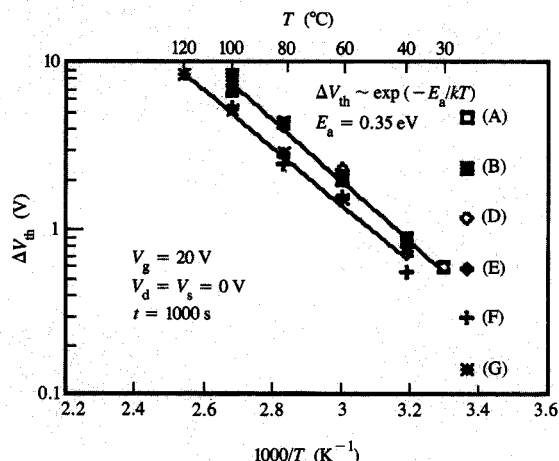


Figure 8

ΔV_{th} as a function of temperature for different insulators, yielding a value for the activation energy E_a . For identification of the samples, see Table 1.

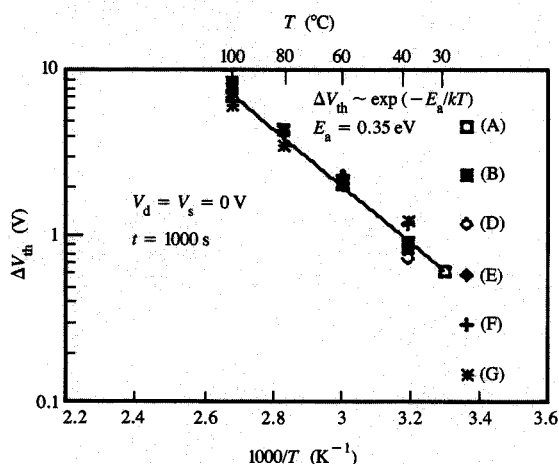


Figure 9

ΔV_{th} as a function of temperature for different insulators. V_g of 20 V is applied to samples A, B, D, and E, but V_g of 24 V is applied to samples F and G. For identification of the samples, see Table 1.

the one for the TFT with SiN_x or $\text{SiN}_x/\text{SiO}_x$ insulator, as shown in Figure 6. As a result, the magnitude of the a-Si band bending was eliminated when $+V_g$ was applied. In order to normalize to this effect, a V_g of 19 V was

applied only to sample F. This applied gate voltage was determined by adding the differential value between the V_{th} of sample F and the other ones before stress, namely 4 V, to a V_g of 15 V. Consequently, all V_{th} shifts then had the same value, as shown in Figure 7. This suggested that it makes little difference in the V_{th} shift whether the insulator is SiN_x or SiO_x .

• Dependency of the V_{th} shift on temperature

As shown in Figure 8, a V_g of 20 V was applied to samples A, B, D, E, F, and G, at 80°C, for 1000 s. Recall that samples A, B, D, and E were fabricated with a SiN_x layer. On the other hand, samples F and G were fabricated with only a SiO_x layer. In addition, samples A, D, and F were fabricated with an AO film, but samples B, E, and G were fabricated without this film. As a result, the V_{th} shifts of samples A, B, D, and E were equivalent, but the V_{th} shifts of samples F and G were smaller than any of the others, as has been described above. However, the activation energy of all of the samples had the same value of 0.35 V. To normalize to the effect of a high V_{th} before stress, a V_g of 24 V was applied to samples F and G at 80°C for 1000 s. This applied gate voltage was also determined by adding the differential value between the V_{th} shifts of samples F and G and the other ones before stress, namely 4 V, to a V_g of 20 V. Consequently, all V_{th} shifts then had the same value, as shown in Figure 9. This suggested that the AO film has no relation to the activation energy of the V_{th} shift and that it makes no difference whether the insulator is SiN_x or SiO_x .

• Dependency of the V_{th} shift on V_g

Figure 10 shows the V_{th} shift when V_g between 5 and 30 V was applied to samples A, B, D, E, F, and G at 80°C for 1000 s. Recall that samples A, B, D, and E were fabricated with a SiN_x layer. On the other hand, samples F and G were not fabricated with a SiN_x layer, but with a SiO_x layer. In addition, samples A, D, and F were fabricated with an AO film, but samples B, E, and G were fabricated without this film. As a result, the V_{th} shifts of all of the samples were equivalent, except that the V_{th} shifts of samples F and G were smaller, as has been described in the previous section. In order to normalize to the effect of the higher V_{th} before stress, the V_{th} shift curves of samples F and G were redrawn by setting the X-axis not to V_g but to $V_{g\text{SiO}_x}$, which is equal to $V_g - 4$, as shown in Figure 11. Consequently, all V_{th} shifts then had the same value. This suggests that the V_{th} shift does not depend on V_g and that it makes no difference whether the insulator is SiN_x or SiO_x .

Conclusion

The results of these BTS experiments show that the AO film makes no contribution to the V_{th} shift and that it

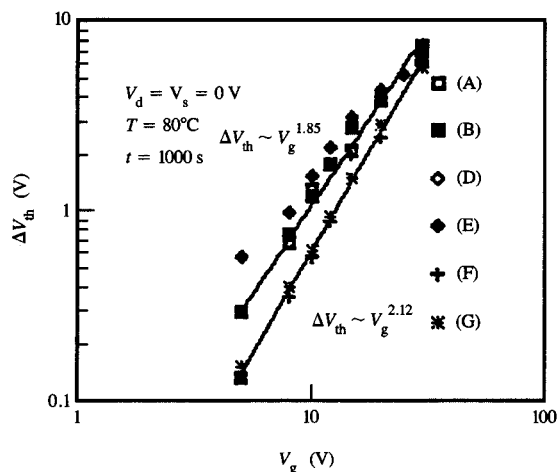


Figure 10

ΔV_{th} as a function of gate voltage for different insulators, yielding a value for the parameter α . For identification of the samples, see Table 1.

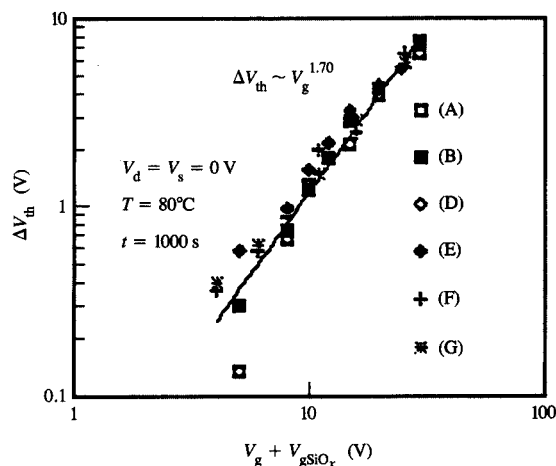


Figure 11

ΔV_{th} as a function of gate voltage for different insulators. The X-axis of samples A, B, D, and E corresponds to V_g , but the X-axis of samples F and G corresponds to $V_g - 4$. For identification of the samples, see Table 1.

makes little difference whether the insulator is SiN_x or SiO_x . The latter fact may be interpreted in two ways. One is that electrons injected into the insulator by the a-Si:H band bending cause the V_{th} shift, and both SiN_x and SiO_x make the same contribution to the V_{th} shift. That is, these two different gate insulators may have the same charge-transport and trapping mechanism, and thus give rise to the same dependency of the V_{th} shift on stress time, temperature, and gate voltage, as has been described. On the other hand, the creation of the metastable states at the a-Si:H/gate insulator interface could cause the V_{th} shift. Thus, neither SiN_x nor SiO_x makes any contribution to the V_{th} shift, but the a-Si:H/gate insulator interface is the important contributor. These experiments cannot show which theory is consistent with the behavior of the V_{th} shift observed in this work. Therefore, to confirm the mechanism, it is necessary to fabricate a series of a-Si:H TFTs under different growth conditions (temperature, H content, deposition power) and measure the V_{th} shift for each sample. If the results show that the shifts are different, they are due to the a-Si:H/gate insulator interface, not to the gate insulator, whether it is SiN_x or SiO_x . If the results show that the V_{th} shifts are independent of growth conditions, it can be concluded that the V_{th} shift is due to the trapping of injected electrons in the insulator and not to the a-Si:H/gate insulator interface, and that both SiN_x and SiO_x make the same contribution to the V_{th} shift.

References

1. M. J. Powell, "Charge Trapping Instabilities in Amorphous Silicon-Silicon Nitride Thin-Film Transistors," *Appl. Phys. Lett.* **43**, 597 (1983).
2. C. van Berkel and M. J. Powell, "Resolution of Amorphous Silicon Thin-Film Transistor Instability Mechanisms Using Ambipolar Transistors," *Phys. Lett.* **51**, 1094 (1987).
3. M. J. Powell, C. van Berkel, I. D. French, and D. H. Nicholls, "Bias Dependence of Instability Mechanisms in Amorphous Silicon Thin-Film Transistor," *Appl. Phys. Lett.* **51**, 1242 (1987).
4. A. R. Hepburn, J. M. Marshall, C. Main, M. J. Powell, and C. van Berkel, "Metastable Defects in Amorphous-Silicon Thin-Film Transistors," *Phys. Rev. Lett.* **56**, 2215 (1986).
5. N. Ibaraki, M. Kigoshi, K. Fukuda, and J. Kobayashi, "Threshold Voltage Instability of a-Si:H TFTs in Liquid Crystal Displays," *J. Non-Cryst. Solids* **115**, 138 (1989).
6. Albert V. Ferris-Prabhu, "Charge Transfer by Direct Tunneling in Thin-Oxide Memory," *IEEE Trans. Electron Devices* **ED-24**, 524 (1977).
7. D. L. Staebler and C. R. Wronski, "Optically Induced Conductivity Changes in Discharge-Produced Hydrogenated Amorphous Silicon," *J. Appl. Phys.* **51**, 3162 (1980).

Received September 23, 1991; accepted for publication March 5, 1992

Yukinobu Fujimoto IBM Japan, Display Technology, 1623-14, Shimotsuruma, Yamato-shi, Kanagawa-ken 242, Japan (JL03471 at YMTVM1, JL03471 at YKTVMT). Mr. Fujimoto is a characterization engineer working with

amorphous silicon thin-film-transistor technology at the IBM Japan Yamato Laboratory. In 1982 he received the B.E. degree from the University of Tokyo. He subsequently joined IBM Japan, and has since been engaged in the characterization of amorphous silicon thin-film-transistor TFT/LCD devices. Mr. Fujimoto is a member of the Japanese Physical Society and the Japan Society of Applied Physics.